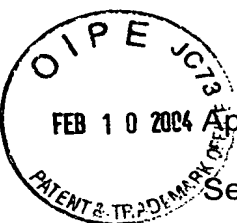


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Applicants: Yasushi KOUBUCHI, ET AL.

Serial No.: 10/619,039

Filed: July 14, 2003

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, AND
FABRICATION PROCESS AND DESIGNING METHOD
THEREOF

Group: 2811

Examiner of parent: Lee

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.97 & 1.98

Mail Stop DD
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

February 10, 2004

Sir:

In the matter of the above-identified application, applicants are submitting herewith a copy the document listed in the attached form equivalent to form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted before the mailing date of a first office action on the merits.

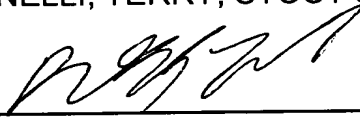
Each of the documents listed on the attached form equivalent to Form PTO 1449 is in the English language.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus Deposit Account No. 01-2135 (501.36127CC) please credit any excess fees to such deposit account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



Ralph T. WEBB
Registration No. 33,047

RTW/dmw
(703) 312-6600

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609: Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.